

Atty Docket No. JCLA8533-D2

Serial No. 10/755,042

AMENDMENTSIn The Claims:

## Claims 1-29. (canceled)

30. (currently amended) A chip package structure comprising:

at least a die having a first active device and a second active device; and  
a metal layer deposited over said die and extending to a place under which there is no die,  
wherein a signal is suited for being transmitted from said first active device to said second active  
device through said metal layer.

~~\_\_\_\_\_ a substrate having a surface;~~  
~~\_\_\_\_\_ a plurality of dies, wherein each die has an active surface, a backside that is~~  
~~opposite to the active surface, and a plurality of metal pads located on the active surface, whereas~~  
~~the backside of each die is adhered to the surface of the substrate;~~  
~~\_\_\_\_\_ a thin film circuit layer located over the substrate and the die and having an~~  
~~external circuitry, wherein the external circuitry is electrically connected to the metal pads of the~~  
~~die and extends to a region outside the active surface of the die, the external circuitry has a~~  
~~plurality of bonding pads located on a surface layer of the thin film circuit layer and each~~  
~~bonding pad is electrically connected to a corresponding metal pad of the die; and~~  
~~\_\_\_\_\_ at least one passive device positioned inside or on the thin film circuit layer,~~  
~~wherein the passive device is selected from a group consisting of an inductor, a wave guide, a~~  
~~filter, and a micro electronic mechanical sensor (MEMS).~~

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31. (currently amended) The structure in claim 30, wherein multiple of said the dies perform same functions.

32. (currently amended) The structure in claim 30, wherein multiple of said the dies perform different functions.

33. (currently amended) The structure in claim 30 further comprising a substrate under said die. ~~wherein the dies have an internal circuitry and a plurality of active devices located on the active surface of the die, and the internal circuitry is electrically connected to the active devices, whereas the internal circuitry contains the metal pads.~~

34. (currently amended) The structure in claim 30-33 further comprising a dielectric layer over said die, said metal layer deposited on said dielectric layer and electrically connected to said die through at least a via in said dielectric layer. ~~wherein a signal from one of the active devices is transmitted to the external circuitry via the internal circuitry, and from the external circuitry back to other of the active devices via the internal circuitry.~~

35. (currently amended) The structure in claim 30-34, wherein said die has at least a thin-film circuit layer electrically connected to said first active device and said second active device, said metal layer deposited over and electrically connected to said thin-film circuit layer, and said metal layer having a thickness greater than that of said thin-film circuit layer. ~~a width, length, or thickness of the traces of the external circuitry is greater than that of the traces of the internal circuitry to reduce RC delay.~~

36. (currently amended) The structure in claim 30, wherein said metal layer comprises a ground bus or a power bus. ~~the external circuitry further comprising a power/ground bus.~~

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37. (currently amended) The structure in claim 30 further comprising a dielectric layer on said metal layer., ~~wherein the thin film circuit layer comprising at least a patterned wiring layer and a dielectric layer, the dielectric layer is located over the substrate and the die, and the patterned wiring layer is located over the dielectric layer, whereas the patterned wiring layer is electrically connected to the metal pads of the die through the dielectric layer and forms the external circuitry and the bonding pads of the external circuitry.~~

38. (currently amended) The structure in claim 30-37 further comprising a plurality of said dies, said metal layer electrically connecting said dies., ~~wherein the dielectric layer has a plurality of thru holes, and the patterned wiring layer is electrically connected to the metal pads of the die via the thru holes.~~

39. (currently amended) The structure in claim 30-38 further comprising a film layer around said die, and said metal layer further extending over said film layer., ~~wherein a via metal is located inside each thru hole, and the patterned wiring layer is electrically connected to the metal pads of the die via the via metal.~~

40. (currently amended) The structure in claim 39 further comprising a substrate under said die and under said film layer., ~~wherein the patterned wiring layer and the via metal form the external circuitry.~~

**Claims 41-42. (canceled)**

43. (currently amended) The structure in claim 40-39, wherein said substrate comprises metal. ~~the passive device is formed, partly or wholly, by a part of the patterned wiring layer.~~

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44. (currently amended) The structure in claim 40-37, wherein said substrate comprises silicon, ~~a material of the dielectric layer is selected from a group consisting of polyimide, benzocyclobutene, porous dielectric material, and stress buffer material.~~

45. (currently amended) The structure in claim 39-30, wherein said film layer comprises polymer, ~~the thin film circuit layer comprising a plurality of patterned wiring layers and a plurality of dielectric layers, in which the patterned wiring layers and dielectric layers are alternately formed and the patterned wiring layers are electrically connected to the neighboring patterned wiring layers through the dielectric layer, one of the dielectric layers is formed between the thin film circuit layer and the substrate, the patterned wiring layer that is closest to the substrate is electrically connected to the metal pads of the dies through the dielectric layer that is closest to the substrate, where the patterned wiring layer that is furthest away from the substrate contains the bonding pads.~~

46. (currently amended) The structure in claim 39-45, wherein said film layer comprises silicon, ~~each of the dielectric layers has a plurality of thru holes, by which each of the patterned wiring layer is electrically connected the neighboring patterned wiring layers, where the patterned wiring layer that is closest to the silicon substrate is electrically connected to the metal pads of the dies through the thru holes that are closest to the substrate.~~

47. (currently amended) The structure in claim 39-46, wherein said film layer has a surface coplanar with an active surface of said die, ~~a via metal is located in each thru hole, by which the patterned wiring layers are electrically connected to the neighboring patterned wiring~~

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layers, where the patterned wiring layer that is closest to the substrate is electrically connected to the metal pads of the die via the via metal that is closest to the substrate.

48. (currently amended) The structure in claim 30-47 further comprising a substrate, wherein said substrate has at least a cavity accommodating said die, said substrate having a surface coplanar with an active surface of said die, and said metal layer further extending over said surface of said substrate. , wherein the patterned wiring layers and the via metal form the external circuitry.

**Claims 49-51. (canceled)**

52. (currently amended) The structure in claim 48-45, wherein said substrate comprises silicon. a material of the dielectric layer is selected from a group consisting of polyimide, benzocyclobutene, porous dielectric material, and stress buffer material.

**Claim 53 (canceled)**

54. (currently amended) The structure in claim 30, wherein said die has an active surface, said metal layer deposited over said active surface of said die. ~~the substrate comprising a silicon layer and a heat conducting layer formed overlapping, the surface of the substrate is provided by a surface of the heat conducting layer, which is closer to the silicon layer, and the silicon layer has a plurality of openings that penetrate through the silicon layer and is meant to form the inwardly protruded areas, allowing the dies put into the inwardly protruded areas.~~

55. (currently amended) The structure in claim 30-54 further comprising a passive device deposited at a place under which there is no die. , wherein a thickness of the silicon layer is approximately equal to a thickness of the dies.

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56. (currently amended) The structure in claim 30 further comprising a passive device deposited over said die. a filling layer located between the a surface of the substrate and the thin-film circuit layer and surrounding the peripheral of the die, and a surface of the filling layer is planar to the active surface of the die.

57. (currently amended) The structure in claim 30-56 further comprising a passive device electrically connected to said die, wherein said passive device comprises a capacitor, a resistor, an inductor, a filter, a wave guide, or a micro electronic mechanical sensor (MEMS). ; wherein a material of the filling layer is selected from a group consisting of epoxy and polymer.

58. (currently amended) The structure in claim 30 further comprising at least a bump deposited over said die or at a place under which there is no die, wherein said bump comprises solder. further comprising a passivation layer located on top of the thin-film circuit layer and exposing the bonding pads.

59. (currently amended) The structure in claim 30 further comprising at least a bump deposited over said die or at a place under which there is no die, wherein said bump comprises gold. a plurality of bonding points located on the bonding pads.

60. (currently amended) The structure in claim 30-59 comprising only one said die. ; wherein the bonding points are solder balls.

**Claims 61-140 (canceled)**

141. (new) A chip package structure comprising:  
a substrate;

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at least a die joined with said substrate, and having a first active device and a second active device; and

a metal layer deposited over said die, wherein a signal is suited for being transmitted from said first active device to said second active device through said metal layer.

142. (new) The structure in claim 141, wherein multiple of said dies perform same functions.

143. (new) The structure in claim 141, wherein multiple of said dies perform different functions.

144. (new) The structure in claim 141 further comprising a dielectric layer over said die, said metal layer deposited on said dielectric layer and electrically connected to said die through at least a via in said dielectric layer.

145. (new) The structure in claim 141, wherein said die has at least a thin-film circuit layer electrically connected to said first active device and said second active device, said metal layer deposited over and electrically connected to said thin-film circuit layer, and said metal layer having a thickness greater than that of said thin-film circuit layer.

146. (new) The structure in claim 141, wherein said metal layer comprises a ground bus or a power bus.

147. (new) The structure in claim 141 further comprising a dielectric layer on said metal layer.

148. (new) The structure in claim 141 further comprising a plurality of said dies joined with said substrate, said metal layer electrically connecting said dies.

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149. (new) The structure in claim 141 further comprising a film layer deposited around said die and over said substrate.

150. (new) The structure in claim 149, wherein said film layer comprises polymer.

151. (new) The structure in claim 149, wherein said film layer comprises silicon.

152. (new) The structure in claim 149, wherein said film layer has a surface coplanar with an active surface of said die.

153. (new) The structure in claim 141, wherein said substrate comprises metal.

154. (new) The structure in claim 141, wherein said substrate comprises silicon.

155. (new) The structure in claim 141, wherein said substrate has at least a cavity accommodating said die, said substrate having a surface coplanar with an active surface of said die.

156. (new) The structure in claim 141, wherein said die has an active surface and a backside, said backside of said die joined with said substrate, and said metal layer deposited over said active surface of said die.

157. (new) The structure in claim 141 further comprising a passive device deposited at a place under which there is no die.

158. (new) The structure in claim 141 further comprising a passive device deposited over said die.

159. (new) The structure in claim 141 further comprising a passive device electrically connected to said die, wherein said passive device comprises a capacitor, a resistor, an inductor, a filter, a wave guide, or a micro electronic mechanical sensor (MEMS).

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160. (new) The structure in claim 141 further comprising at least a bump deposited over said die or at a place under which there is no die, wherein said bump comprises solder.

161. (new) The structure in claim 141 further comprising at least a bump deposited over said die or at a place under which there is no die, wherein said bump comprises gold.

162. (new) The structure in claim 141 comprising only one said die.